REMARKS

By this amendment, claims 2-4, 7, 9 and 10 are canceled without prejudice or disclaimer, claims 1, 5, 6, 8, 11, 18, 25 and 29 are amended, and claims 31-33 are added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Claim Objection

Claim 4 was objected to because it does not further limit the claim from which it depends. This rejection is moot. By this Amendment, claim 4 has been canceled.

35 U.S.C. §112, 2nd paragraph, Rejection

Claims 2, 3, 5, 7, 9, 10 and 29 are rejected under 35 U.S.C. §112, 2nd paragraph, as being indefinite. This rejection is moot. By this Amendment, claims 2, 3, 7, 9 and 10 have been canceled. Additionally, the any features of these claims which have been included in claim 1 have been amended to resolve this basis of rejection. Furthermore, claims 5 and 29 have been amended in a manner which is believed to resolve this basis of rejection.

35 U.S.C. §101 Rejection

Claims 1-30 are rejected under 35 U.S.C. §101 as failing to accomplish a practical result and/or as being directed to non-statutory subject matter.

This rejection is moot. By this Amendment, claims 1, 11, 18 and 25 have been amended in a manner which is believed to resolve this basis of rejection consistent with

MPEP 2106. In particular, claims 1, 11 and 18 have been amended to recite that the method is implemented with computer program code (which can be either software or hardware) and hardware. Furthermore, claim 25 has been amended to recite that the upper layer and the lower layer are arranged on a multi-layer structure of a semiconductor device implementing the circuit design source data. Such language clearly imparts tangible features to the claims.

35 U.S.C. §102(b) Rejection

Claims 1-5, 9, 11-13, 16, 18-20, 23 and 25-28 are rejected under 35 U.S.C. §102(b) as being anticipated by an Article entitled "Post-route optimization for improved yield using a rubber-band wiring model" by SU et al. (1997). This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because SU fails to teach each and every element of the claims.

In particular, independent claim 1 recites, *inter alia,*

wherein the method one of:
introduces jogs in wires of one layer arranged above wires of another layer;
introduces segments of wrong-way wiring in wires of one layer arranged above wires of another layer;
increases a space of minimum-spaced wires over a wider structure;

forms a dummy hole in an incompatible structure component of a first layer of the problem structure to reduce manufacturing defects of a structure component in a second layer of the problem structure; and widens a trench of a lower layer of the problem structure under at least one wire of an upper layer of the problem structure.

Additionally, independent claim 11 recites, *inter alia,*

determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer; and if so performing at least one of:

increasing a space between the two minimum-spaced wires of the upper layer in a region over the dishing-prone structure of the lower layer,

forming a dummy hole in a wide wire under the space between the two minimum-spaced wires; and

widening a trench between two wide wires under the space between the two minimum-spaced wires

Furthermore, independent claim 18 recites, *inter alia,*

forming a dishing-prone structure on a lower layer;
forming two minimum-spaced wires over the dishing-prone structure on an upper layer;
increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure;
if the dishing-prone structure includes a wide wire, inserting a space for a dielectric island in the wide wire under at least one wire of the two minimum-spaced wires; and
if the dishing-prone structure includes a narrow trench between two wide wires, widening the narrow trench under of the space between the two minimum-spaced wires.

Still further, independent claim 25 recites, *inter alia,*

an upper layer comprising multiple minimum-spaced wires;
a lower layer comprising a dishing-prone structure, wherein the multiple minimum-spaced wires of the upper layer are disposed over the dishing-prone structure of the lower layer;
an increased space between at least two wires of the multiple minimum-spaced wires in a region over the dishing-prone structure;
a dummy hole in the wide wire under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a wide wire; and
a widened region of the narrow trench under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a narrow trench between two wide wires.

Applicants submit that SU does not disclose, or even suggest, at least these features.

Applicants acknowledge, for example, that SU discloses a program which can increase wire spacing in an effort to design circuits having minimized bridging faults and minimized critical area (see Sections 2.0 and 6.0). However, the Examiner has not identified any language in SU which discloses or suggests that jogs in wires of one layer arranged above wires of another layer are introduced, or that segments of wrong-way wiring in wires of one layer arranged above wires of another layer are introduced, or that a space of minimum-spaced wires over a wider structure is increased, or that a dummy hole in an incompatible structure component of a first layer of the problem structure is formed to reduce manufacturing defects of a structure component in a second layer of the problem structure, or that a trench of a lower layer of the problem structure under at least one wire of an upper layer of the problem structure is widened (claim 1). While it is true that SU explains that the disclosed program can span multiple layers (see left-side bottom paragraph of page 701), SU is not concerned with preventing a manufacturing defect on one layer by modifying another layer according to the method of claim 1.

On page 5 of the instant Office Action, the Examiner argues that SU teaches determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer. Applicants disagree. While it is true that SU aims to increase wire spacing in circuit design (see Section 3.0), SU is entirely silent with regard to minimum-spaced wires, much less, those of an upper layer that pass over a dishing-prone structure. SU also fails to even mention that if it is determined that at

least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer, performing at least one of: increasing a space between the two minimum-spaced wires of the upper layer in a region over the dishing-prone structure of the lower layer, or forming a dummy hole in a wide wire under the space between the two minimum-spaced wires, or widening a trench between two wide wires under the space between the two minimum-spaced wires (claim 11).

The Examiner additionally argues on page 6 of the instant Office Action that SU teaches forming a dishing-prone structure on a lower layer, forming two minimum-spaced wires over the dishing-prone structure on an upper layer, increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure, if the dishing-prone structure includes a wide wire, inserting a space for a dielectric island in the wide wire under at least one wire of the two minimum-spaced wires, and if the dishing-prone structure includes a narrow trench between two wide wires, widening the narrow trench under of the space between the two minimum-spaced wires (claim 18). Applicants disagree. Again, while it is true that SU aims to increase wire spacing in circuit design (see Section 3.0), SU is entirely silent with regard to minimum-spaced wires, much less, those of an upper layer that pass over a dishing-prone structure.

The Examiner also argues on page 7 of the instant Office Action that SU teaches an upper layer comprising multiple minimum-spaced wires, a lower layer comprising a dishing-prone structure, wherein the multiple minimum-spaced wires of the upper layer are disposed over the dishing-prone structure of the lower layer, an increased space between at least two wires of the multiple minimum-spaced wires in a region over the dishing-prone structure, a dummy hole in the wide wire under at least one wire of the

multiple minimum-spaced wires if the dishing-prone structure includes a wide wire, and a widened region of the narrow trench under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a narrow trench between two wide wires (claim 25). Applicants disagree. Again, SU aims to increase wire spacing in circuit design (see Section 3.0) but is entirely silent with regard to minimum-spaced wires, much less, those of an upper layer that pass over a dishing-prone structure.

Thus, Applicants respectfully submit that independent claims 1, 11, 18 and 25, and claims which depend therefrom are allowable.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(b) should be withdrawn.

New Claims are also Allowable

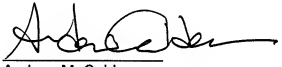
Applicants submit that the new claims 31-33 are allowable over the applied art of record. Specifically, claims 31-33 depend from claim 1 which is believed to be allowable. Moreover, claims 31-33 recite a combination of features which are clearly not disclosed or suggested by the applied art of record. Accordingly, Applicants respectfully request consideration of these claims and further request that the above-noted claims be indicated as being allowable.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to

issue. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0456** (Burlington).

Respectfully submitted,
Paul H. BERGERON et al.



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